REMARKS

The Examiner has (1) rejected claims 1-6, 8, 9, 13, and 14 as obvious over Estakhri (U.S. Pat. No. 6,081,878) in view of Koh (U.S. Pat. Pub. No. 2003/1067376); (2) rejected claim 7 as obvious over Estakhri in view of Koh and USB2.0; (3) rejected claims 10 and 11 as obvious over Estakhri in view of Koh and Yamazaki (U.S. Pat. No. 5,699,297); (4) rejected claim 12 as obvious over Estakhri in view of Koh, Yamazaki, and Hasbun (U.S. Pat. No. 5,581,723). In this Response, Applicants amend claims 1 and 13. Based on the amendments and arguments contained herein, Applicants believe this case to be in condition for allowance.

Applicants amend claim 1 to clarify that the master control unit is further arranged to "simultaneously erase a section of memory space of each of the at least two NAND flash memory units". Clear basis for this amendment is found at least at para. 55 of the application as published by the Office. The amended claim 1 now requires the master control unit to erase a section of memory space of each of the at least two NAND flash memory units simultaneously (in time). In contrast to the amended claim 1, Estakhri does not disclose that the controller (Figure 5: 510) of the memory system (Figure 5: 500) erases sections of memory spaces of the first and the second flash memory chip (Figure 5: 670, 672) simultaneously in time.

In fact column 19 line 18 to column 20 line 45 and the various waveforms shown in Figure 14 (reproduced below) of Estakhri actually teach one of ordinary skill in the art that the controller 510 erases the first chip 670 and the second flash memory chip 672 sequentially in time. Specifically Estakhri teaches that a section of the first flash memory chip 670 is erased at time E9, whereas a section of the second flash memory chip 672 is erased at a later time E11.

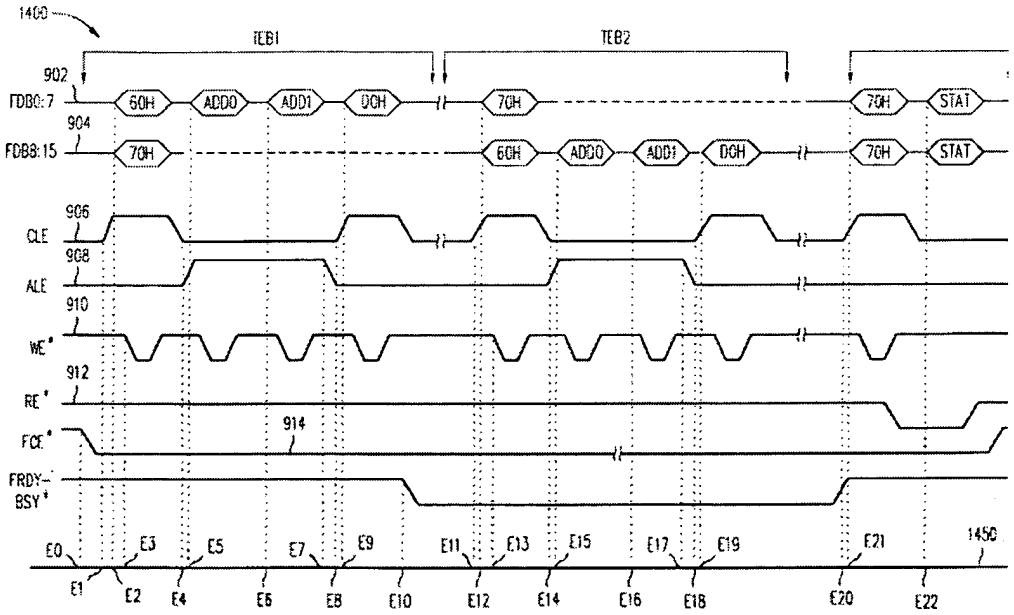

FIG. 14

Although there is a typographical error in Estakhri (column 20 lines 30-34 should have instead referred to the second waveform 904 and not the first waveform 902, which was explained in column 19 lines 56-63), column 20 lines 35-45 nevertheless makes it clear that the section of the first flash memory chip 670 is erased during the time interval **TEB1** whereas the section of the second flash memory chip is erased during the (later) time interval **TEB2**; see Figure 14 also. Accordingly respective sections of the first and the second flash memory chip 670; 672 are sequentially – and **not** simultaneously – erased by the controller 510.

In the Final Office Action, the Examiner has asserted that Estakhri's CLE signal that is sent to the first and second flash memory chips falls within the scope of the previous claim 1 in respect of the feature of the signal being simultaneously transmitted to the at least two NAND flash memory units to cause the erasure. Applicants respectfully submit that the Estakhri's CLE signal does not fall within the scope of claim 1 as amended, since the CLE signal clearly does **not** erase sections of the first and the second flash memory chips simultaneously.

Moreover, and as explained above, Estakhri's controller 510 is **not** suitable for erasing sections of the first and the second flash memory chip simultaneously because it has already been configured to do so sequentially in time. Hence Estakhri's controller also does not fall within the specific wording of the amended claim 1 in respect of the feature of the master control unit being "further arranged to simultaneously erase a section of memory space of each of the at least two NAND flash memory units".

Therefore there is no teaching in Estakhri to lead one of ordinary skill in the art towards the invention of claim 1. By requiring the master control unit to simultaneously erase a section of memory space of each of the at least two NAND flash memory units, embodiments of this invention can advantageously perform faster operations compared with those as performed by the memory system of Estakhri, for example. This might be useful when memory devices are operating at near full capacity so that blocks are available for re-used as soon as they have been erased.

Thus the amended claim 1 is not obvious over Estakhri.

Since Koh does not disclose that the controller (Figure 5: 120) erases sections of the flash memories (Figure 5: 22) simultaneously, the controller 120 is thus not configured – and hence not suitable – for erasing the flash memories 22 simultaneously. Applicants submit that one of ordinary skill in the art faced with the teachings of both Estakhri and Koh would not also have arrived at the invention of claim 1. Accordingly the amended claim 1 is not obvious over the combination of Estakhri and Koh also.

Similar comments also apply to the corresponding method claim, claim 13, as amended, which is thus also patentable over Estakhri and Koh – either alone or in combination. The dependent claims, by virtue of their dependencies at least, are also patentable over the cited documents.

None of the other art of record satisfies the deficiencies of Estakhri and Koh.

CONCLUSION

Applicants respectfully request that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required are hereby authorized to be charged to Conley Rose, PC's Deposit Account No. 03-4729.

Respectfully submitted,

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